Contact Doping of Silicon Wafers and Nanostructures with Phosphine Oxide Monolayers

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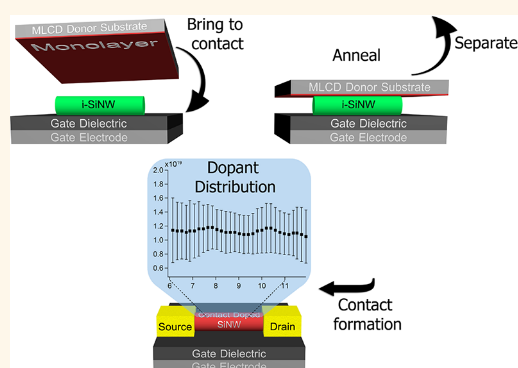
ABSTRACT Contact doping method for the controlled surface doping of silicon wafers and nanometer scale structures is presented. The method, monolayer contact doping (MLCD), utilizes the formation of a dopant-containing monolayer on a donor substrate that is brought to contact and annealed with the interface or structure intended for doping. A unique feature of the MLCD method is that the monolayer used for doping is formed on a separate substrate (termed *donor substrate*), which is distinct from the interface intended for doping (termed *acceptor substrate*). The doping process is controlled by anneal conditions, details of the interface, and molecular precursor used for the formation of the dopant-containing monolayer. The MLCD process does not involve formation and removal of SiO_2 capping layer, allowing utilization of surface chemistry details for tuning and simplifying the doping process. Surface contact doping of intrinsic Si wafers (*i*-Si) and intrinsic silicon nanowires (*i*-SiNWs) is demonstrated and characterized. Nanowire devices were formed using the *i*-SiNW channel and contact doped using the MLCD process, yielding highly doped SiNWs. Kelvin probe force microscopy (KPFM) was used to measure the longitudinal dopant distribution of the SiNWs and demonstrated highly uniform distribution in comparison with *in situ* doped wires. The MLCD process was studied for *i*-Si substrates with native oxide and H-terminated surface for three types of phosphorus-containing molecules. Sheet resistance measurements reveal the dependency of the doping process on the details of the surface chemistry used and relation to the different chemical environments of the P═O group. Characterization of the thermal decomposition of several monolayer types formed on SiO_2 nanoparticles (NPs) using TGA and XPS provides insight regarding the role of phosphorus surface chemistry at the SiO_2 interface in the overall MLCD process. The new MLCD process presented here for controlled surface doping provides a simple yet highly versatile means for achieving postgrowth doping of nanometer scale structures and interfaces.



KEYWORDS: silicon · nanowires · monolayer doping · surface chemistry

Controlled doping of semiconductors is challenging in the context of recent top-down device architectures as well as for architectures based on bottom-up building blocks, such as semiconducting nanowires (NWs).[1,2] Sharp junctions and localized dopant profiles are key for fine control of the electronic structure and nanoscale properties.[3−8] Specifically, controlled surface doping may play an important role in implementing current semiconductor devices such as FinFETs (fin-shaped field effect transistors) and as an important tool for practical nanowire-based devices and photovoltaic building blocks.[9−16] Conventional doping methods such as ion implantation[17,18] or solid-source diffusion for controlled nanometer scale surface doping is challenging due to limitations such as nanoscale lattice damage, dopant equilibration throughout the nanostructure, and random dopant fluctuations (RDFs).[19−21] In the context of semiconducting NWs, the commonly used *in situ* CVD doping method suffers from several limitations, including nonhomogenous longitudinal dopant distribution resulting from continuous exposure of the growing SiNW to the dopant precursor along the CVD synthesis process.[22−25]

A substantial advance toward surface doping with nanometer scale control was recently introduced by the monolayer doping (MLD) method.[19,20,26−28] Important characteristics of the MLD approach rely on the

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separation of the doping step from the nanoscale building block synthesis, utilization of the substrate interface for placement of potential dopant atoms, and avoiding damage to the crystal lattice that is critical for nanometer scale structures. To achieve this, the intrinsic silicon substrate is reacted to form a monolayer with dopant atoms directly at the pristine semiconductor surface, followed by capping of the dopant-containing monolayer with a SiO_2 layer. The *i*-Si substrate, capped with SiO_2, is thermally annealed at elevated temperatures where decomposition of the monolayer and subsequent dopant diffusion onto the Si lattice and dopant activation take place during the anneal process. This approach was previously used for demonstrating the formation of ultrashallow doping profiles at interfaces of nanostructures and for large-scale areas.[20] Here we present a novel approach for controlled surface doping of silicon wafers and nanometer scale structures that utilize the formation of a dopant-containing monolayer at a separate substrate from the interface or structure intended for doping. In addition, this process does not involve formation and removal of SiO_2 capping layer; we term the method monolayer contact doping (MLCD).

A unique feature of the MLCD method is that a monolayer containing dopant atoms is formed on a separate substrate (termed *donor substrate*) which is distinct from the Si interface intended for doping. The donor substrate with the dopant-containing monolayer is brought to contact directly with pristine *i*-Si substrate or interface intended for surface doping (termed *target substrate*) and annealed using rapid thermal anneal (RTA). During the annealing process, monolayer molecules thermally decompose and dopant atoms originate from the fragmented monolayer diffusion into both the donor and target substrates. The resulting doping in the donor and target substrates is referred to as monolayer doping (MD) and contact doping (CD), respectively (Figure 1). MLCD presents valuable characteristics by further simplification of the surface doping process and compatibility with conventional top-down semiconductor processes as well as bottom-up nanoscale building block synthesis requirements. This is enabled by restriction of the dopant-containing monolayer formation to the donor substrate without exposing the target substrate intended for doping to the surface chemistry process (CD substrate), where the desired circuit architecture or nanoscale structure is present. Furthermore, since MLCD does not require SiO_2 capping, where the fine details of monolayer surface chemistry are obscured, the donor as well as the target surface chemistry can be utilized to fine-tune the doping process and utilize the distinct diffusion and surface properties of SiO_2 *versus* Si.

RESULTS AND DISCUSSION

MLCD surface doping processes were studied using *i*-Si substrates with native oxide (15 ± 2 Å) and for *i*-Si substrates after removal of the native oxide layer to form H-terminated interface. Three types of phosphorus-containing molecules, diphenylphosphine oxide (P1), triphenylphosphine oxide (P2), and tetraethylmethylenediphosphonate (P3), were used to form monolayers on the donor *i*-Si substrate with native oxide for studying the role of surface chemistry in the MLCD process.

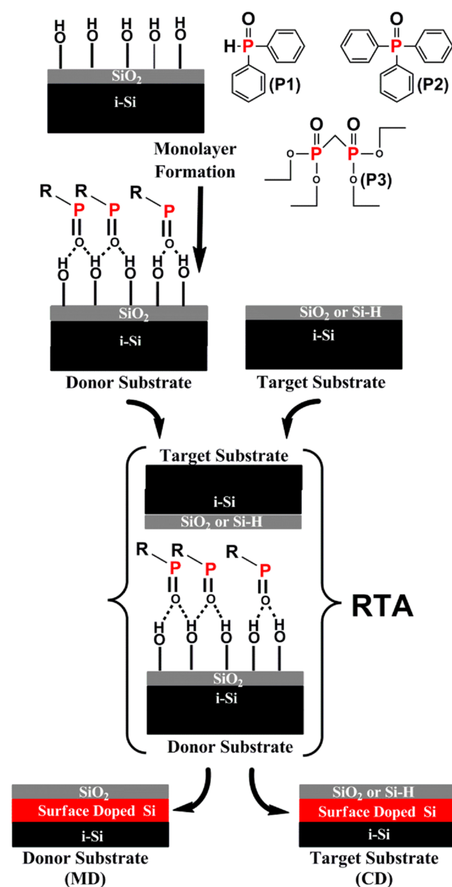

Figure 1. Monolayer contact doping (MLCD) process schematics. A monolayer containing dopant atoms is formed on a *donor substrate* using P1, P2, or P3 precursor molecules. The donor substrate and pristine *i*-Si substrate, *target substrate*, are brought to contact and annealed using rapid thermal anneal (RTA). During the annealing process, monolayer molecules thermally decompose and dopant atoms originate from dopant diffusion into both donor and target substrates. The resulting surface doping in the donor and target substrates is referred to as MD and CD, respectively.

For clarity of the discussion that follows, we define the notation applicable for the MLCD process: The donor substrate on which the dopant-containing monolayer is formed and undergoes rapid thermal anneal is termed monolayer doping, the target substrate that is in contact with the MD substrate during the thermal anneal is termed contact doping (Figure 1).

The details of the target substrate interface layer are specified by a subscript, CD_{Si-H} or CD_{Native}, for H-terminated and native oxide layer at the *i*-Si CD substrate, respectively.

The utilization of phosphine oxide–SiO_2 surface chemistry is advantageous for exploring the MLCD process since the dopant-containing molecules are

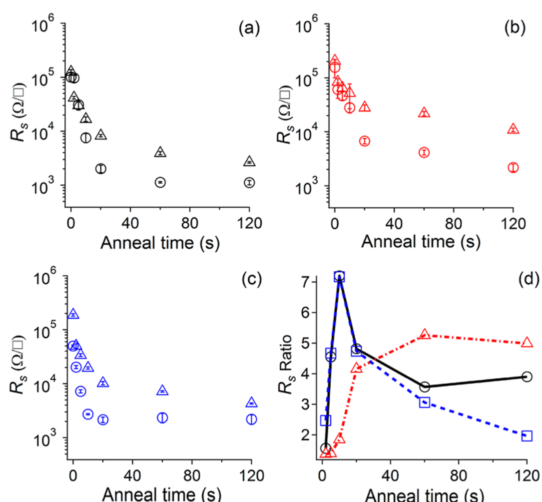

Figure 2. Sheet resistance (R_s) *vs* anneal time for phosphorus contact doping of *i*-Si(100) obtained for CD_{Native} (△) and for CD_{Si-H} (○). Molecular precursors used for the MLCD process: (a) P1, (b) P2, and (c) P3, annealed at 1005 °C. (d) Sheet resistance ratios $R_s^{NativeOxide}/R_s^{Si-H}$ as function of annealing time for contact doping by P1 (○), P2 (△), and P3 (□).

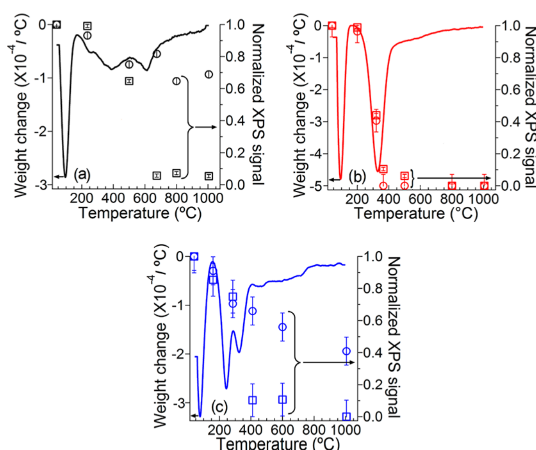

Figure 3. Differential thermal gravimetry profiles (DTG) and X-ray photoelectron spectroscopy (XPS). $P2_p$ (○) and $C1_s$ (□) normalized signals for (a) P1, (b) P2, and (c) P3 monolayers formed on SiO_2 nanoparticles annealed at various temperatures.

formed directly[29,30] at the native oxide of the donor substrate without an additional molecular linker that may affect the subsequent diffusion of dopant atoms during the thermal decomposition and annealing steps. Monolayer formation on the donor substrate was confirmed by spectroscopic ellipsometry and X-ray photoelectron spectroscopy (XPS) measurements. Four-point probe measurements were used to obtain sheet resistance values (R_s) following RTA process with P1, P2, and P3 monolayer formed on the donor substrate for various anneal times at 1005 °C (Figure 2a–c). For MLCD processes performed with P1, P2, and P3 monolayers, R_s values show a sharp decrease with anneal time, both for CD_{Si-H} and for CD_{Native} processes, similar to previously reported results for the MLD method.[19] The initial rapid decrease of R_s values with anneal time followed by minor decrease in R_s for longer anneal times is expected for the limited source diffusion of dopant atoms defined by the monolayer source.[19] For MLCD, the initial surface dose of dopant atoms is defined by the molecular details such as molecular footprint and monolayer surface coverage formed at the donor substrate interface, similar to the case for MLD.[19,20] As expected, R_s values obtained for CD_{Si-H} processes are systematically lower compared to R_s values obtained for CD_{Native} processes. These results suggest that the thin native oxide layer functions as a barrier layer, reducing the incorporation of dopant atoms to the underlying Si substrate, but does not completely block the dopant diffusion process, as expected for thin native oxide layer.[31] The surface doping and sharp decrease in R_s values for CD_{Si-H} using the MLCD process do not require SiO_2 capping layer formation and removal, typically part of the previously reported MLD method.[19] This distinct characteristic of the MLCD process may be useful for applications where further processing steps are required. The doping efficiency for the P1-MLCD process carried out at 1005 °C was estimated using previously reported analysis.[19] Considering a molecular footprint of 1 nm^2 for P1 molecules, we estimate doping efficiencies of 55 and 7% for CD_{Si-H} and CD_{Native} target substrates, respectively. Figure 2d presents a comparison of the $R_s^{NativeOxide}/R_s^{Si-H}$ ratios obtained for CD_{Native} and CD_{Si-H} for P1, P2, and P3-MLCD processes for various anneal times. Qualitatively, for both P1 and P3, a sharp initial increase of the ratio $R_s^{NativeOxide}/R_s^{Si-H}$ is reaching maxima at $t \sim 10$ s, followed by a decrease of the ratios for longer anneal times. In contrast, for P2, a steady increase of the ratio $R_s^{NativeOxide}/R_s^{Si-H}$ is obtained until $t \sim 60$ s, with no significant change of the ratio values for longer anneal time. Namely, two different types of profiles are revealed by considering the $R_s^{NativeOxide}/R_s^{Si-H}$ ratios for the different phosphorus-containing monolayers studied here.

To better understand the different $R_s^{NativeOxide}/R_s^{Si-H}$ profiles obtained for P2 as compared to those of P1 and P3 molecular precursors, and the interaction of phosphorus species with the oxide layer, SiO_2 NPs were reacted with the respective molecular precursors P1, P2, and P3 and were thermally annealed. Thermogravimetric analysis (TGA) and X-ray photoelectron spectroscopy (XPS) analyses were performed for SiO_2 NPs reacted with P1, P2, and P3 monolayers for various anneal temperatures. $C1_s$ and $P2_p$ XPS signals were used to quantify the changes in carbon and phosphorus content accompanying the thermal anneal process and monolayer decomposition for each type of monolayer reacted with SiO_2 NPs and annealed at various temperatures corresponding to changes in the differential thermal gravimetry (DTG) profiles (Figure 3). P1 and P3 monolayers show similar behavior with sharp decrease in $C1_s$ signal with increasing anneal temperature and partial decrease in the $P2_p$ signal for

elevated temperatures, with significant retention of phosphorus in the SiO_2 matrix up to 1005 °C. In contrast, XPS results for the P2 monolayer show concomitant decrease occurring for both the $C1_s$ and $P2_p$ signals with almost complete depletion of carbon and phosphorus at anneal temperatures above 400 °C. Overall, the TGA-XPS results show that phosphorus retention in the SiO_2 matrix varies significantly for the different types of monolayers studied here, with retention of ~70% for P1, ~0% for P2, and ~40% for P3 of the phosphorus species for 1005 °C. In addition, carbon species were removed completely from the SiO_2 matrix for NPs reacted with P1, P2, and P3 and annealed at 1005 °C. The differences in phosphorus retention in the SiO_2 NP matrix obtained from the TGA-XPS results may be attributed to the different chemical environment of the P═O group for the different types of molecular precursors used. The P═O functional group of P1, P2, and P3 precursors can form H-bond interactions with the oxide interface promoting the monolayer formation.[29] In addition to H-bond interactions of the P═O group and polar silanol (−Si−OH) groups at the oxide interface, for both P1 and P3 precursors, covalent interactions at the oxide interface may form, as well. The different modes of surface interactions and the different chemical environments of the P═O group for the different precursors studied here may affect the type of phosphorus species formed during the thermal anneal and monolayer decomposition process, thereby affecting the phosphorus species retention in the SiO_2 matrix.[32] Both P1 and P3 precursors resulted in significant retention of phosphorus in the SiO_2 matrix at high anneal temperatures, while P2 resulted in complete loss of the phosphorus species at high anneal temperatures. The two distinct types of phosphorus retention profiles obtained from the TGA-XPS data may be related to the two distinct types of $R_s^{NativeOxide}/R_s^{Si-H}$ profiles. For P1 and P3, the maxima observed for $R_s^{NativeOxide}/R_s^{Si-H}$ ratio for $t \sim 10$ s may result from two opposite processes occurring for the short and long anneal times. Initially, for short anneal times, preferential incorporation of dopant atoms occurs for the Si−H-terminated surface, CD_{Si-H}, compared to the native oxide interface, for CD_{Native}. However, for longer anneal times, the incorporation of phosphorus species that were retained in the SiO_2 layer is more significant as compared to the Si−H interface. This result in decrease in the $R_s^{NativeOxide}/R_s^{Si-H}$ value for longer anneal times compared to the peak value for $t \sim 10$ s, resulting in the characteristic R_s ratio profile. In contrast, for the P2 monolayer, a steady increase of R_s ratio related to the preferred incorporation into the CD_{Si-H} surface as compared to the CD_{Native} surface until $t \sim 60$ s because of the thin oxide layer. For longer anneal times, however, no significant change of the $R_s^{NativeOxide}/R_s^{Si-H}$ value is observed since phosphorus species were not retained in the SiO_2 layer for this case, as

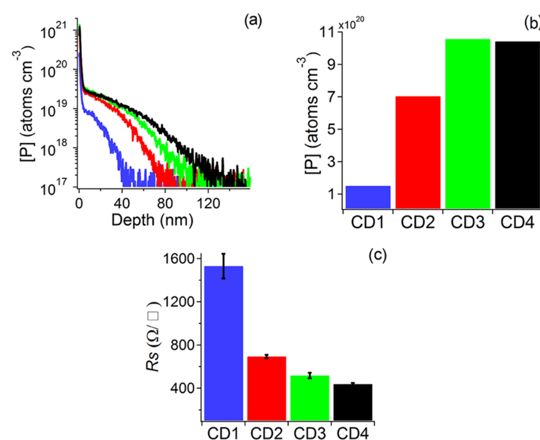

Figure 4. Multiple contact doping process for Si−H-terminated Si wafer, CD_{Si-H}^n, for $n = 1-4$. (a) TOF-SIMS phosphorus concentration profiles. (b) Phosphorus surface concentration. (c) Sheet resistance values obtained by four-point probe measurements. Target substrate was treated with HF to form the Si−H interface, and donor substrate with native oxide was reacted with P1 to form a monolayer. Each MLCD process was carried out with freshly formed P1 monolayer on the donor substrate, brought to contact with the Si−H-terminated acceptor substrate, and annealed for 60 s at 1005 °C.

revealed by the TGA-XPS data obtained for SiO_2 NPs reacted with P2. This result is currently under further study using solid-state ^{31}P NMR spectroscopy expected to provide an additional insight regarding the details of phosphorus species and interactions involved with the SiO_2 matrix for the different surface chemistries and anneal processes presented here.

Further, repeated contact doping processes were studied for the P1 monolayer formed at the donor substrates and applied to form CD_{Si-H}^n target substrates, where $n = 1-4$ indicates the contact doping process repetition number. For each CD_{Si-H}^n process, a fresh donor substrate with a P1 monolayer was used with the same target substrate for n times. Time of flight secondary ion mass spectroscopy (TOF-SIMS) measurements were performed to quantify the doping profile of the P atom for CD_{Si-H}^n processes. TOF-SIMS results show a systematic increase of phosphorus concentrations for consecutive processes (Figure 4a,b). For the first CD process ($n = 1$, CD_{Si-H}^n), a surface concentration of phosphorus of ~1.5×10^{20} atoms/cm^3 is obtained, close to the solid solubility limit at 1005 °C,[33] with sharp decrease to 1.0×10^{18} atoms/cm^3 at a depth of ~30 nm. For the consecutive CD_{Si-H}^n processes, surface concentrations of 7.0×10^{20}, 11×10^{20}, and 10×10^{20} atoms/cm^3 are obtained for $n = 2, 3$, and 4, respectively (Figure 4b). R_s values for CD_{Si-H}^n decrease for $n = 1-4$ follow the same trend obtained from the TOF-SIMS phosphorus-doping profiles (Figure 4c). The most significant increase in surface concentration and decrease of R_s value is obtained for $n = 2$, while for $n = 3$ and 4, a moderate increase in surface concentration and correspondingly moderate decrease in R_s values are obtained, consistent with dopant saturation levels and

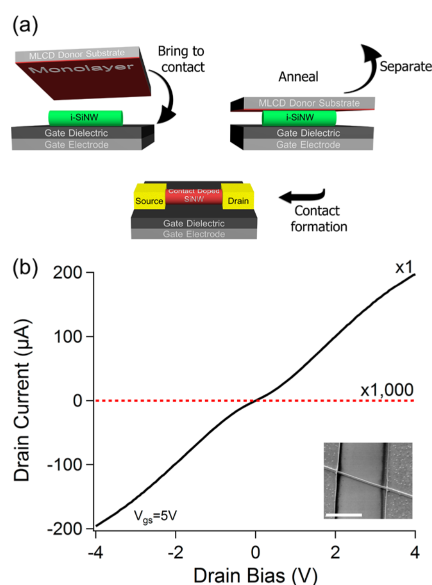

Figure 5. Monolayer contact doping of SiNW devices. (a) Schematic of the MLCD process for NW device formation. (b) Source−drain current *vs* voltage curves for *i*-SiNW device (dotted line) and for phosphorus contact-doped with MLCD 1005 °C, 20 s process (solid line). Inset: SEM micrograph of SiNW device, scale bar 2 μm.

reduced efficiency of dopant incorporation at this high doping regime of >5 × 10^{20} atoms/cm^3.[3,34]

Nanowire Device Formation by MLCD. MLCD was applied to *i*-SiNW to yield phosphorus contact-doped SiNWs followed by two-terminal device fabrication with back-gate electrodes. *i*-SiNWs were grown using chemical vapor deposition, drop-cast on a p^{++}-Si/SiO_2(100 nm)/Si_3N_4(100 nm) substrate, contact-doped using the MLCD process with the P3 monolayer reacted at the donor substrate, and electrically characterized (Figure 5b).

Prior to contact doping, the *i*-SiNW device exhibits a nonactive source−drain channel with ~20 GΩ resistance at 2 V. In contrast, the contact-doped NW device show ~6 orders of magnitude increase in conductivity compared to the intrinsic device, as demonstrated by the *I*−*V* curves with ~20 kΩ resistance at 2 V (Figure 5b). The highly doped device does not show response to the applied gate voltage as expected for the degenerately doped SiNW channel.[19]

Kelvin probe force microscopy (KPFM)[23,24,35,36] was used to measure the longitudinal dopant distribution of contact-doped SiNW devices with channel length of ~10 μm between S−D symmetric electrodes using a conductive tip. *i*-SiNWs ($d \sim 80$ nm) were doped with a phosphorus−MLCD process (900 °C, 30 s, P3 monolayer) to yield intermediate level doping. Specifically, the contact potential difference (CPD) measured by KPFM is defined as

$$\mathrm{CPD} = -(\Phi_{\mathrm{tip}} - \Phi_{\mathrm{sample}})/q \qquad (1)$$

where Φ_{tip} and Φ_{sample} are the work functions of the tip and sample, respectively, and q is the elementary charge.[37]

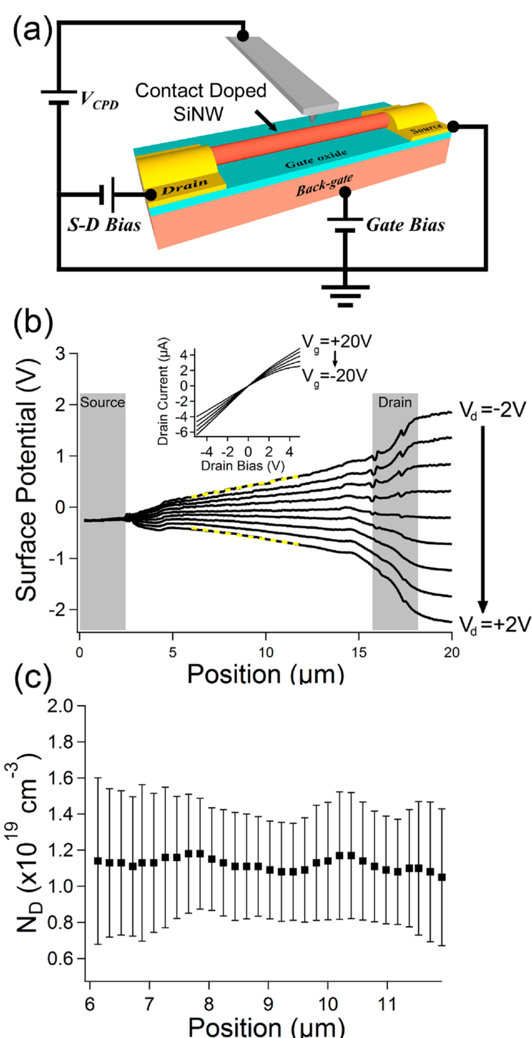

Figure 6. (a) Schematic of KPFM measurements setup. (b) Source−drain current−voltage (*I*−*V*) curves of a single SiNW device for different back-gate biases with respect to the grounded (source) electrode. The yellow dashed lines are a guide for the eye, showing the linearity of the potential profile away from the electrodes. The gray shaded areas represent the electrodes. (c) Local effective doping extracted from KPFM and current measurements.

The sample surface potential is measured by nullifying the contact potential difference (CPD) between the measuring probe (tip) and the sample, thus eliminating any tip-induced band bending.[38]

The KPFM-measured surface potential along a SiNW under applied voltages ranging from −2 V to +2 V with 0.5 V steps is shown in Figure 6b. For KPFM measurements, voltage was applied by biasing the drain electrode while keeping the source and the back-gate electrodes grounded. The *I*−*V* curves show a linear response around the zero bias, indicating that the Al electrodes form Ohmic contacts to the NW. The decrease in resistivity with the increase in back-gate bias suggests that the NW forms an n-channel device operating in the enhancement mode. The regions in proximity with the metal electrodes show a significant depletion region stemming from the metal−semiconductor contact

potential difference and the applied bias (Figure 6b). Notably, along the central part of the MLCD-doped nanowire channel, away from the depletion regions, the surface potential is linear, as can be seen from the comparison with the dashed line (yellow). A least mean squares analysis of the potential profile showed a good fit to linearity with $R^2 > 0.99$. The linearity of the surface potential demonstrates that the electric field along the wire is constant and, therefore, that the doping concentration along the wire is constant, as well (Figure 6c). These results point at an important characteristic of the MLCD process attributed to the separation of the doping process from the NW CVD synthesis. In contrast, for *in situ* doping of SiNWs such as for NW doping during the CVD growth process, it was demonstrated that non-uniform distribution of dopant atoms is obtained along the NW growth axis.[22] The nonuniformity is the result of the continuous SiNW surface exposure to the PH_3 precursor during the CVD synthesis process.[22-24] This result in a nonlinear potential drop along the biased SiNW as detected by the surface potential measured directly *via* KPFM and by integrating the photocurrent measured by SPCM.[22] The local effective doping, that is, the concentration of ionized dopant atoms, N_D^+, can be extracted from the combination of KPFM and current measurements results.[38] By differentiating the measured surface potential, $\Phi_{sample}(x)$, with respect to the distance along the wire, the local electric field can be calculated. Then, by using the measured current for the bias applied, N_D^+ is given by

$$N_D^+(x) = \frac{J}{q\mu_n(N_D^+)\dfrac{d\Phi_{sample}(x)}{dx}} \qquad (2)$$

where J is the current density and μ_n (N_D^+) is the electron mobility for phosphorus-doped silicon, with dopant concentration of N_D^+. Using eq 2, a doping concentration of $(1 \pm 0.5) \times 10^{19}$ cm^{-3} is obtained with assumed mobility of 110 cm^2/(V·s) corresponding to the bulk mobility at this concentration.

CONCLUSION

Monolayer contact doping is demonstrated for the controlled and local surface doping of silicon wafers, interfaces, and nanometer scale building blocks. The contact doping method details were studied for phosphorus using different molecular precursors for understanding the molecular details involved in the process. Characterization of the thermal decomposition of the different types of monolayers formed on SiO_2 NPs using TGA and XPS provides insight regarding the role of phosphorus surface chemistry at the SiO_2 interface in the overall MLCD process. Multiple contact doping processes yield high doping levels with surface dopant concentration higher than 5×10^{20} cm^{-3}. Dopant profiles depths of 30−40 nm were demonstrated, and ultrashallow profiles of less than 10 nm are achievable using short anneal times. Contact doping of SiNWs with controlled dopant concentration is demonstrated and applied for the formation of SiNW-based devices. KPFM results show high dopant uniformity along the nanowire compared to conventional *in situ* doping of SiNWs. Separation of the doping process from the synthesis of nanostructures and separation of the surface chemistry monolayer formation process required for the dopant placement to a separate substrate are key characteristics of the new method. We expect MLCD to open new possibilities for nanometer scale device formation that was difficult to obtain based on conventional *in situ* doping schemes. The MLCD process may be extended for additional dopants such as boron and arsenic by using suitable molecular precursors and surface chemistry. The method may also be applicable for doping of other semiconductors or metal oxides.

MATERIALS AND METHODS

Substrate Cleaning. Intrinsic silicon substrates (*i*-Si ⟨100⟩) were cleaned by dipping in hot Piranha solution (3:1 by volume of concentrated H_2SO_4 and 30% H_2O_2) for 15 min. The substrates were then washed with triple distilled water (TDW). The Piranha-cleaned substrates were further cleaned with $H_2O/H_2O_2/NH_4OH$ (5:1:1; 30% H_2O solution, ~27% NH_4OH solution) solution kept in an ultrasonic bath for 8 min at 60 °C. After washing with TDW, the substrates were dipped in ethanol and dried with a nitrogen stream. The substrates were then kept in an oven at 115 °C for 10 min. For each monolayer formation reaction, freshly cleaned substrates were used.

Caution: Piranha solutions are extremely strong and dangerous oxidizing agents and should be used with extreme caution. May explode in contact with organic solvents.

Monolayer Formation on Si/SiO_2 Wafers. Monolayer formation reactions were performed in 100 mL screw-capped bottles. Freshly cleaned i-Si ⟨100⟩ substrates (~2 cm^2) and 20 mL of the precursor solution in mesitylene were loaded in the bottles and tightly sealed. The reactions were then carried out at 100 °C for 2 h. After completion of the reaction, the *i*-Si ⟨100⟩ substrates were removed from the precursor solution and washed by dipping in mesitylene (×3) and dichloromethane (×3) and dried by blowing nitrogen. The freshly prepared *i*-Si substrates with monolayers were used as the donor for the MLCD process.

Monolayer Formation on SiO_2 NPs. Monolayer formation reactions were performed in 20 mL screw-capped bottles; 0.1 g of 15 nm SiO_2 NPs and 5 mL of the precursor solution in mesitylene were loaded in the bottles and tightly sealed. The reactions were then carried out at 100 °C for 2 h. After completion of the reaction, the monolayer-containing SiO_2 NPs were removed from the precursor solution by centrifugation, the supernatant phase was discarded, and the NPs were washed in mesitylene and redispersed (×3), followed by *n*-hexane (×2), and finally dried at 115 °C.

Rapid Thermal Annealing. AnnealSYS MicroAS system was used for RTA processes. Prior to the anneal step, the chamber was purged with Ar and then evacuated to a pressure of 10^{-2} Torr. Heating was carried out at 83 °C/s. Prior to each MLCD process, a blank anneal process was performed to remove dopant residue from the instrument chamber.

Nanowire Growth. SiNWs were grown in a custom-built CVD system using the vapor–liquid–solid mechanism. During the NW growth process, temperature was set to 440 °C, 35 Torr pressure, 30 min duration, 50 sccm H_2, and 2 sccm SiH_4 gas flow. Glass slides were used as substrates for NW CVD growth. Glass slides were cleaned by O_2 plasma (30% power 1 min); then poly-L-lysine solution, 0.1% (w/v) in H_2O (Sigma), was applied to the substrate for 5 min followed by rinse with DI water and dried under N_2 stream. Then, 80 nm AuNP solution (Ted Pella, Inc.) was placed on the poly-L-lysine-coated glass substrate for 2 min, followed by thorough rinse with DI water, and dried under N_2 stream.

Nanowire Devices. SiNWs with a diameter of 80 nm were used for fabricating electrical devices. NW suspensions in ethanol were freshly prepared by mild sonication and immediately used for drop-cast on a Si(p^{++})/SiO_2(100 nm)/Si_3N_4(100 nm) wafer. Nanowire devices were fabricated by photolithography using AZ nLOF2020 photoresist and electrical contacts formed by metal evaporation for source and drain electrodes (100 nm Ni or 120 nm Al). Prior to the metal evaporation step, oxygen plasma was applied to remove residual resist and organic contaminations and a 3 s wet buffered oxide etch to remove the native oxide layer. Lift off was performed by immersing in *N*-methyl-2-pyrrolidone (NMP) at 80 °C. Global back-gate contact to the substrate was used for bias voltage. Electrical measurements were conducted using a semiconductor parameter analyzer (Agilent B1500A). KPFM measurements were conducted using a Dimension Edge AFM system (Bruker AXS) and a Pt–Ir-coated tip, in a controlled nitrogen environment glovebox (less than 5 ppm H_2O), in the "lift mode", where the forward scan is a "tapping mode" topography measurement and in the backward scan the tip is raised to a constant 50 nm height above the topography trajectory and measures the CPD. Channel lengths for electrical characterization and KPFM were $\sim$2 and $\sim$10 μm, respectively.

Sheet Resistance Measurement. Sheet resistance was measured using four-point probe setup (Jandel, RM3-AR). All samples were treated by dipping in 5% HF solution, DI water, and isopropyl alcohol and dried under N_2 stream before measurement.

SIMS Measurements. SIMS measurements were carried out using the IonTof TOFSIMS5 system. Samples were analyzed in negative mode, monitoring $^{30}Si^-$ and $^{31}P^-$ secondary ions, using a 25 KeV Bi^+ primary beam for analysis and a 0.5 KeV Cs^+ sputtering ion beam, both at an incidence angle of 45°. The analyzed area size was 80 μm $\times$ 80 μm. Stylus profilometry was used for determining the depth of sputtered craters and for depth profile calibration. Concentrations of P in the Si substrate were calculated using a relative sensitivity factor (RSF) determined from a standard sample for P.

TGA Experiments. Thermogravimetric analysis (TGA) was performed using a Mettler-Toledo TGA/SDTA 851e system. Differential thermal gravimetry profiles (DTG) were calculated from the data using STARe software. Experiments were performed from 40 to 1005 °C at a constant ramp rate of 10 °C/min, under a 50 mL/min flow of dry nitrogen.

Monolayer Characterization. Monolayer formation was characterized by variable-angle spectroscopic ellipsometry (VASE) using a VB-400 spectroscopic ellipsometer (J.A. Woolam Co.). Ellipsometry measurements were performed on a Si(100) substrate with native oxide (oxide thickness 1.8 nm), yielding 7 $\pm$ 1 and 4 $\pm$ 1 Å for P1 and P3, respectively.

XPS data were collected with a Kratos Axis Ultra X-ray photoelectron spectrometer. Spectra were acquired with monochromatic Al Kα radiation. XPS analysis was performed for monolayers formed on Si(100) substrate with thermal oxide to avoid XPS Si plasmon signal overlaying the $P2_p$ signal.[39] P1 resulted in 134.5 and 285.8 eV binding energies for $P2_p$ and $C1_s$, respectively. P3 resulted in 134.7 and 286.2 eV binding energies for $P2_p$ and $C1_s$ binding energies, respectively. The formation of monolayer by P2 was confirmed by literature values as previously reported.[29]

Conflict of Interest: The authors declare no competing financial interest.

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